application and Keeth '307 were, at the time the invention was made, owned by the same person.[1]

In any event, Keeth '307 actually *supports*, rather than contradicts, Applicant's arguments made in the Appeal Brief. Keeth '307 teaches an open bit line architecture memory cell of $6F^2$ or smaller feature size that employs switching of digit line levels to eliminate the signal to noise ratio problems of prior designs. Keeth '307 also considers the use of the folded bit line architecture, but teaches that folded bit line architectures resulted in a memory cell with a minimum size of $8F^2$. Keeth '307, 1:36-43. Thus, Keeth '307 is consistent with Aoki in teaching that, conventionally, a folded bit line architectural or configuration cannot achieve a $6F^2$ memory cell size. The teachings of Aoki, and Keeth are important *objective* evidence of knowledge known to persons of ordinary skill in the art *at the time* of the present invention. From the Examiner's impermissible hindsight view, the combination of a folded bit line arrangement and a $6F^2$ memory cell is obvious. However, the objective evidence, set forth in Aoki and Keeth '307, indicates that persons of ordinary skill in the art recognized at the time of the present invention was made that the minimum memory cell size of folded bit line architectures was $8F^2$. The difference between the $6F^2$ and $8F^2$ memory cell sizes is significant, as a space savings of about 25% can be achieved using the $6F^2$ memory cell size. *See* Aoki, 2:14-16 ("[T]he layout of the conventional open bit line configuration has an advantage over the folded bit line configuration in that the cell area can be reduced to 75%."). Thus, from the *objective* evidence set forth in Aoki and Keeth '307, it is clear that persons of ordinary skill in the art considered using the open bit line architecture when trying to achieve space savings. To that end, Aoki describes "an improved layout of open bit line configuration" (Aoki, 2:24-27), and Keeth '307 describes a

[1] The introduction of new references Mori (U.S. Patent No. 6,028,784) and Mueller (U.S. Patent No. 5,864,496) is also improper.

"[d]igit line design using an open architecture memory cell of 6 square feature area ($6F^2$) or smaller feature size and switching of the digit line levels to eliminate the signal to noise ratio problems of the past" (Keeth, 3:11-14).

From the evidence provided by Keeth and Aoki, it is clear that a person of ordinary skill in the art *at the time of the present invention* would not have been motivated to combine the teachings of Aoki and Chu to achieve the claimed invention. Instead, such persons of ordinary skill in the art would have been led to using improved layout designs of open bit line arrangements to achieve $6F^2$ or smaller feature sizes of memory cells. Because there is no motivation or suggestion to combine reference teachings of Aoki and Chu in the manner proposed by the Examiner, it is respectfully submitted that the Examiner has failed to establish a *prima facie* case of obviousness. *See* MPEP § 2143 at 2100-124, 125 (to establish a *prima facie* case of obviousness, there must be some suggestion or motivation, even in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings). The Examiner has failed to cite to any objective evidence, except for the Examiner's own un-supported conclusion, that would provide a suggestion or motivation to achieve $6F^2$ memory cell areas in a folded bit line configuration.

A prior art reference must be considered in its entirety, including portions that would lead away from the claimed invention. *See* MPEP § 2141.03 at 2100-122. Here, it is clear that Aoki would lead a person of ordinary skill in the art away from the claimed invention. Aoki criticizes folded bit line arrangements as being space inefficient, noting that the layout of the conventional open bit line configuration has an advantage over a folded bit line configuration and that the cell area can be reduced to 75%. Aoki, 2:14-16. Aoki expressly considered the possibility of both folded and open bit line configurations in its background section, but Aoki discarded the use of a

folded bit line arrangement because of its space inefficiency as compared to an open bit line arrangement. Thus, a person of ordinary skill in the art looking to the teachings of Aoki and Chu would not have been motivated to achieve the subject matter of the claimed invention.

The Examiner argued that the "main issue in this application is one of the dimensions and/or scaling of Folded Bit Line memory structures." Examiner's Answer at 6. The Examiner cited to MPEP § 2144.04, and the references cited in that section, as holding that differences in size dimensions would not be sufficient to patentably distinguish over the prior art. Note that the *In re Rose*, 220 F.2d 459, 105 U.S.P.Q. 237 (C.C.P.A. 1955) case cited by the MPEP section held that claims reciting that lumber packages that require handling by a lift truck were not sufficient to patentably distinguish over prior art that teaches packages of size and weight that can be lifted by hand. The *In re Rose* case is inapposite here, as the present claims do not relate to reducing the size of packages such that lifting can be lifted by hand versus by lift truck. Here, the claims are directed to memory cells each having an area of about $6F^2$, in which bit lines are coupled to sense amplifiers in a folded bit line configuration, *inter alia*. The objective evidence of the prior art cited, including Aoki, is that conventional folded bit line configurations could not achieve a minimum dimension of $6F^2$, despite the benefits that can be derived from using the combination of a $6F^2$ memory cell size in a folded bit line configuration.

The *In re Rinehart*, 531 F.2d 1048, 189 U.S.P.Q. 143 (C.C.P.A. 1976), case cited by the Examiner addressed the patentability of claims reciting "commercial scale production" and "commercial scale quantities." Again, the holding of this case does not apply to the subject matter of the present claims. *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 U.S.P.Q. 777 (Fed. Cir. 1984), another case cited by the Examiner, addressed dimensional limitations that do not specify a device that performed or operated any differently from the prior art teachings.

However, that is not the case here, as the $6F^2$ storage cell recited in the claims would clearly lead to improved memory device performance, including reduced signal line length to reduce signal losses and reduced memory device size to achieve increased manufacturing efficiency and reduced costs.

A case more on point is *In the Matter of the Application of Ehhreich*, 590 F.2d 902, 200 U.S.P.Q. 504 (C.C.P.A. 1979), which held that prior art references did not render obvious a particle size limitation because the prior art references taught away from the claimed particle size in the formation of coatings, gaskets, or caulking compositions. *In the Matter of the Application of Ehhreich*, 590 F.2d at 908-909. There is no *per se* rule that size limitations are to be given no patentable weight. As is the case in the present application, the *Ehhreich* case also involved prior art that references led persons of ordinary skill in the art *away* from using the subject invention. *See also In re Pearson,* 494 F.2d 1399, 1404, 181 U.S.P.Q. 641 (C.C.P.A. 1974) (holding that the Examiner committed error in asserting that it would be obvious to use a smaller particle size in land plastering operations, noting that the prior art would suggest use of a larger particle size instead of a smaller particle size).

In view of the foregoing, it is respectfully requested that the final rejections be reversed.

V. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: May 7, 2004

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CLAIMS ON APPEAL

1. A semiconductor device, comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line configuration, each bit line including a first level portion and a second level portion; and

active area lines, transistors being formed in the active area lines and electrically coupling corresponding memory cells to corresponding first level bit lines.

2. The semiconductor device of claim 1, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

3. The semiconductor device of claim 2, wherein a column pitch of each memory cell is 2F.

4. The semiconductor device of claim 1, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

5. The semiconductor device of claim 4, wherein the second level portion of each bit line is formed over each capacitor.

6. The semiconductor device of claim 1, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions,

the semiconductor device further comprising contacts between the bit lines and active area lines formed in the slanted portions.

7. The semiconductor device of claim 6, wherein the active area lines are generally straight and the bit lines extend in a wavy pattern.

8. The semiconductor device of claim 6, wherein the bit lines are generally straight and the active area lines extend in a wavy pattern.

9. The semiconductor device of claim 6, each bit line having a first portion on a first side of a corresponding active area line, a second portion on a second side of the corresponding active area line, and a third portion on the first side of the active area line.

10. The semiconductor device of claim 6, wherein the bit lines extend along generally the same direction as the active area lines so that the bit lines and active area lines intersect at predetermined locations.

11. A memory device comprising:
memory cells each having an area of about $6F^2$;
sense amplifiers;
bit lines coupled to the sense amplifiers in a folded bit line arrangement;
active area lines; and
transistors formed in the active area lines and electrically coupling corresponding memory cells to corresponding bit lines.

12. The memory device of claim 11, wherein each bit line has a first level portion and a second level portion, each transistor electrically coupling a corresponding memory cell to a first level portion of a corresponding bit line.

13. The memory device of claim 12, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

14. The memory device of claim 12, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

15. The memory device of claim 14, wherein the second level portion of each bit line is formed over each capacitor.

16. The memory device of claim 11, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions.

17. The memory device of claim 11, wherein each pair of bit lines is coupled to one side of a corresponding sense amplifier.

18. A method of making a memory device, comprising:
forming memory cells each having an area of about $6F^2$;
forming sense amplifiers;
coupling bit lines to the sense amplifiers in a folded bit line arrangement;
forming transistors in active area lines; and
the transistors electrically coupling corresponding memory cells to corresponding bit lines.

19. A method of making a memory device, comprising:
forming memory cells each having an area of about $6F^2$;
forming sense amplifiers;
coupling bit lines to the sense amplifiers in a folded bit line arrangement;
forming transistors in active area lines;
the transistors electrically coupling corresponding memory cells to corresponding bit lines;
forming each bit line of a first level portion and a second level portion; and

coupling each transistor to the first level portion of the corresponding bit line.

20. The method of claim 19, further comprising:

vertically twisting each pair of bit lines at one or more predetermined locations; and

transitioning the bit lines in the pair between the first level portion and the second level portion at each twist.

21. The method of claim 20, further comprising forming a capacitor of each memory cell over the first level portion of each bit line.

22. The method of claim 21, further comprising forming the second level portion of each bit line over the capacitor.

23. The semiconductor device of claim 1, wherein in the folded bit line arrangement a pair of bit lines is coupled to a same side of each corresponding sense amplifier.

24. The memory device of claim 11, wherein in the folded bit line arrangement a pair of bit lines is coupled to a same side of each corresponding sense amplifier.

25. The method of claim 18, wherein coupling the bit lines to the sense amplifiers in the folded bit line arrangement comprises coupling each pair of bit lines to a same side of each corresponding sense amplifier.